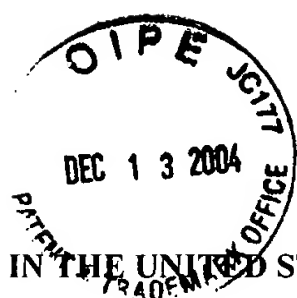


Docket No.: 50090-332



PATENT

AF/2829  
IPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Response Under 37 CFR 1.116 - Expedited Procedure

: Customer Number: 20277

Hisaya MORI, et al.

: Confirmation Number: 4507

Application No.: 09/927,368

: Group Art Unit: 2829

Filed: August 13, 2001

: Examiner: J. M. Hollington

For: APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT

Mail Stop AF

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is a Request for Reconsideration in the above-identified application.

☐  
☐  
☒

No additional fee is required.

Applicant is entitled to small entity status under 37 CFR 1.27

Also attached: Terminal Disclaimer and Petition for Extension of Time

The fee has been calculated as shown below:

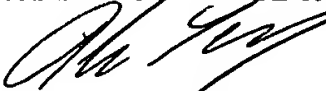
	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	11	20	0	\$50.00 =	\$0.00
Independent Claims	2	3	0	\$200.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$120.00
Terminal Disclaimer					\$130.00
Total of Above Calculations					\$250.00

☒ Please charge my Deposit Account No. 500417 in the amount of \$250.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

  
Alexander V. Yampolsky  
Registration No. 36,324

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
Phone: 202.756.8000 SAB/AVY/dlb  
Facsimile: 202.756.8087  
Date: December 13, 2004

Please recognize our Customer No. 20277 as our  
correspondence address.

Docket No.: 50090-332



Corres. and Mail  
**BOX AF**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Hisaya MORI, et al.

RESPONSE UNDER 37 CFR 1.116  
EXPEDITED PROCEDURE

Application No.: 09/927,368

Filed: August 13, 2001

Customer No.: 20277  
Confirmation No.: 4507

Group Art Unit: 2829

Examiner: J. M. Hollington

Title: APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED  
CIRCUIT

**REQUEST FOR RECONSIDERATION UNDER 37 CFR 1.116**

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This Request is submitted in response to the Office Action mailed August 12, 2004.